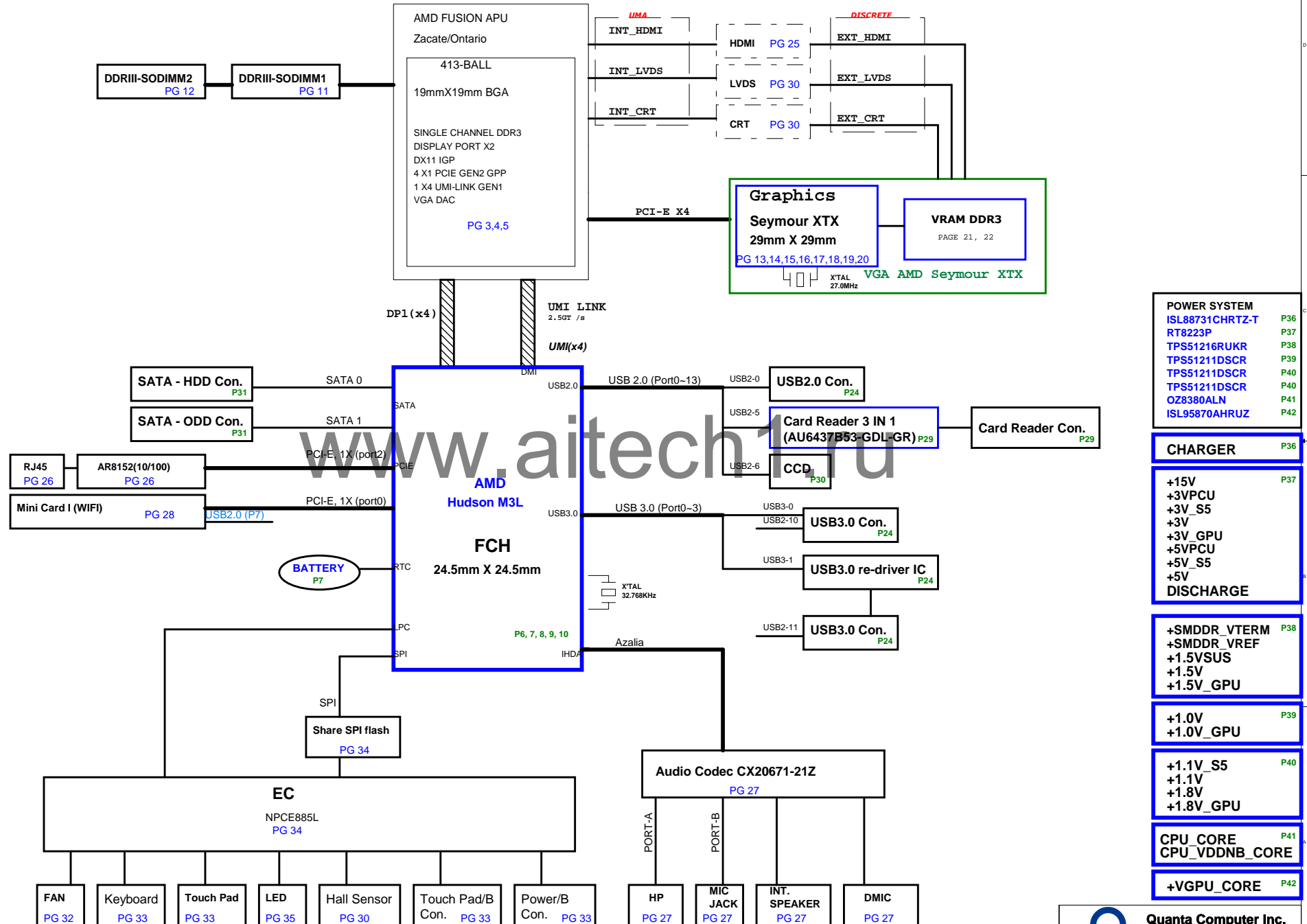


14" BY7D Brazos 2.0 Block Diagram

PCB STACK UP






LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT



PAGE	DESCRIPTION	BOI FUNCTIONS
1	Schematic Block Diagram	
2	POWER STAGE & BOI-FUNCTION	
3 - 5	Processor	CPU
6 - 10	FCH	CLG
7	RTC	RTC
11 - 12	DDRIII SO-DIMM	DDR
13 - 20	Seymour XTX(M2)	VGA
21 - 22	VRAM - DDR3	VGA
23	RESERVE	VGA
24	USB Connector	USB
	USB 3.0 Redriver	U3B
	USB Sleep Charger	SLC
25	HDMI comm part	HDM
	CEC	CEC
26	Atheros LAN	LAN
27	Codec (CX20671-21Z)	ADO
28	MINI Card (Wi-Fi & WIMAX)	MNW
29	Card reader	MMC
30	VGA Connector	VGA
	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
31	HDD	HDD
	ODD	ODD
32	Thermal	THC
	FAN	THC
33	KeyBoard	KBC
	TP&FP board	TPD,FPD
	Power SW	PSW
34	EC NPCE885LA0DX	KBC
35	LED	LED
36	CHARGER-ISL88731C	PWM
37	System 3V/5V(TPS51123A)	PWM
38	DDR 1.5V	PWM
39	+1.0V	PWM
40	+1.1V/+1.8V	PWM
41	CPU CORE	PWM
42	GPU	PWM
43	Power Tree	
44	Power Sequence	
45	Change List	

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAINON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAINON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P	S0
+1.8V	+1.8V	MAINON	S0
+1.5VSUS	+1.5V	SUSON	S0~S3
+1.5V	+1.5V	MAINON	S0
+1.1V_S5	+1.1V	+1.1V_DUAL_EN	S0~S5
+1.1V	+1.1V	MAINON	S0
+1V	+1V	MAINON	S0
CPU_CORE	~	VRON	S0
CPU_VDDNB_CORE	~	VRON	S0
+VGPU_CORE		GPU_VRON	S0
+1.8V_GPU	+1.8V	GPU_MAINON	S0
+1V_GPU	+1V	GPU_PG_VV_EN	S0
+3V_GPU	+3.3V	GPU_MAINON	S0
+1.5V_GPU	+1.5V	GPU_MAINON	S0

ITEM	Value Code	FUNCTIONS
1	CEC@	CEC
2	NMP@	LPC Debug Card
3	512M@	VRAM 512M
4	1GCA@	VRAM 1Gb*4(C-die, A-die)
5	1GEB@	VRAM 1Gb*4(E-die, B-die)
6	2G@	VRAM 2Gb
7	AMD@	AMD VRAM
8	Sam@	Samsung VRAM
9	EV@	DISCRETE
10	IV@	UMA
11	ECRT@	DISCRETE CRT
12	ICRT@	UMA CRT
13	EHM@	DISCRETE HDMI
14	IHM@	UMA HDMI
15	U3@	Internal USB 3.0
16	U2@	USB 2.0 (colay W USB 3.0)
17	ULD@	USB Port (Left Down)
18	ULU@	USB Port (Left Up)
19	ULU2@	USB 2.0 Port (Left Up)
20	ULU3@	USB 3.0 Port (Left Up)
21	UR@	USB Port (Right)
22	UR2@	USB 2.0 Port (Right)
23	UR3@	USB 300 Port (Right)

GND PLANE	PAGE
 8769GND	34
 GND	26
 GND	ALL
 ADOGND	27
 Shield_GND	27



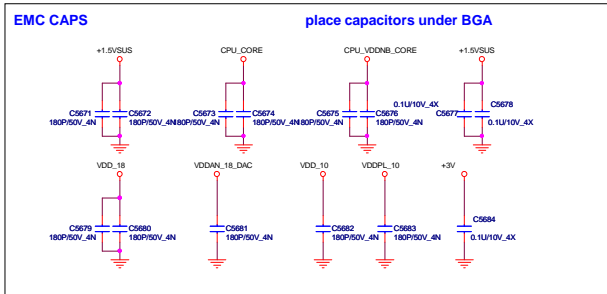
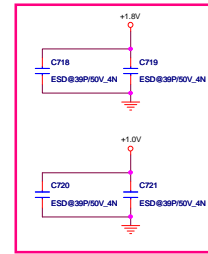
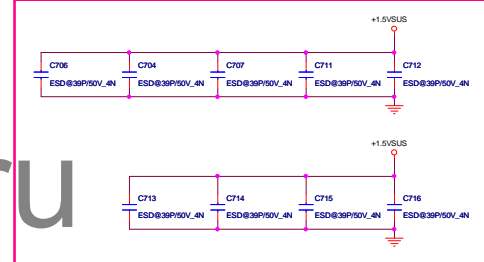
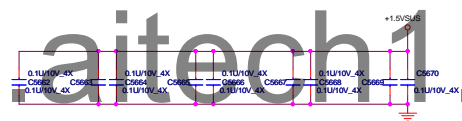
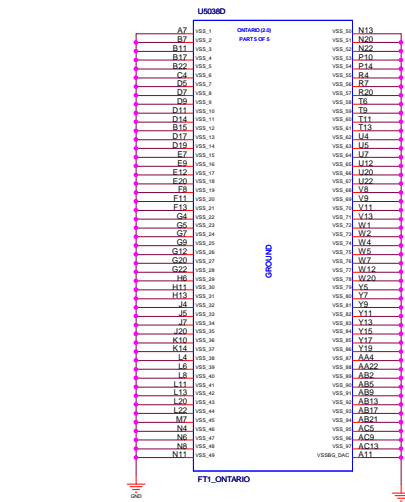


34) APU_PROCHOT#_VDDIO

[illegible]

CPU Thermal sensor HW control

VFIX MODE		VID Override Circuit
SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



For LAN,WLAN



For Dimm



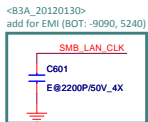
For Lan&WiFi




For Lan&WiFi



For Lan&WiFi



<B3A_20120130>
add for EMI (BOT: -9090, 5240)



The diagram shows a capacitor labeled C601 with a value of E@2200P/50V_4X. It is connected in parallel between the SMB_LAN_CLK signal line and a ground symbol.

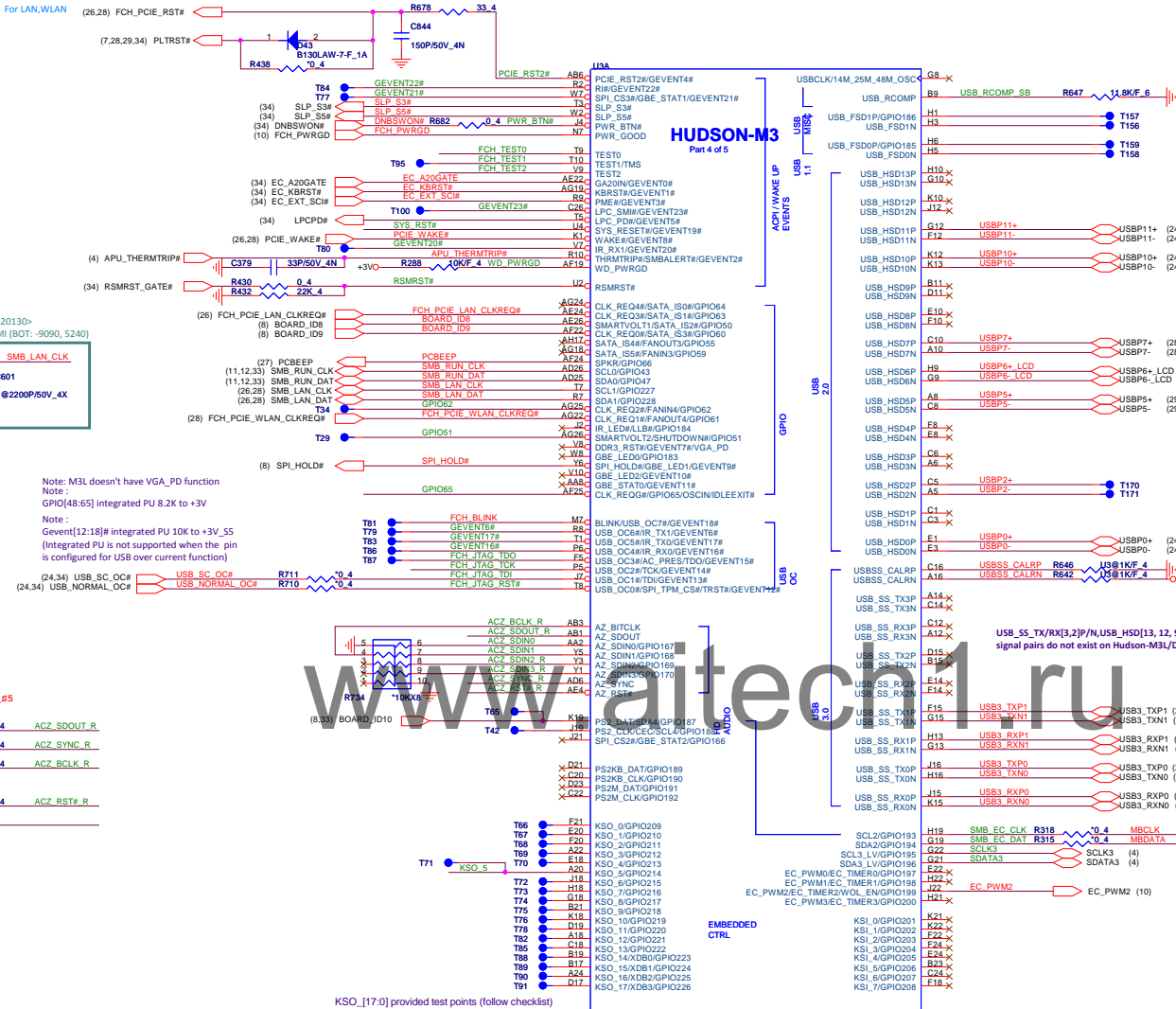
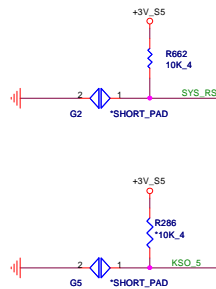
Note: M3L doesn't have VGA_PD function
Note :
GPIO[48:65] integrated PU 8.2K to +3V

Note :
Gevent[12:18]# integrated PU 10K to +3V_5
(Integrated PU is not supported when the p
is configured for USB over current function)

(24,34) USB_SC_OC# USB_SC_OC#
(24,34) USB_NORMAL_OC# USB_NORMAL_OC#

To Azalia

To Azalia



Hudson-M3

KSO_[17:0] provided test points (follow checklist)

EC will Conflict with FCH, did not mount R315&R318

EC	FCH	Device I2C_Device(S)			
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		EEPROM	APU		ALL
I2Ce_3(M)		VGA Thermal			
	I2Cf_3(M)			APU	S5
	I2Cf_1(M)	Lan	WLAN		S5
	I2Cf_0(M)	Dimm	Clk Gen		S0

Note :
USB 2.0 and USB 3.0 signal pair combinations to a single USB 3.0 connector:

- USB_SS_TX/RX1P/N and USB_HSD11P/N
- USB_SS_TX/RX0P/N and USB_HSD10P/N

<Layout Note>
USB P/N pairs with trace lengths up to 10"

- WLAN
- CCD on LVDS
- Card Reader

USB2.0 debug port
(Left Down)

USB3.0 Port 2

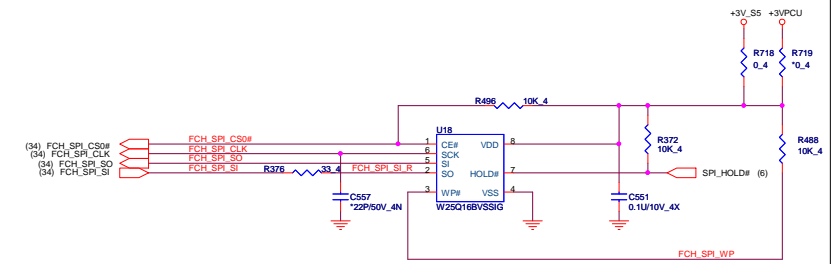
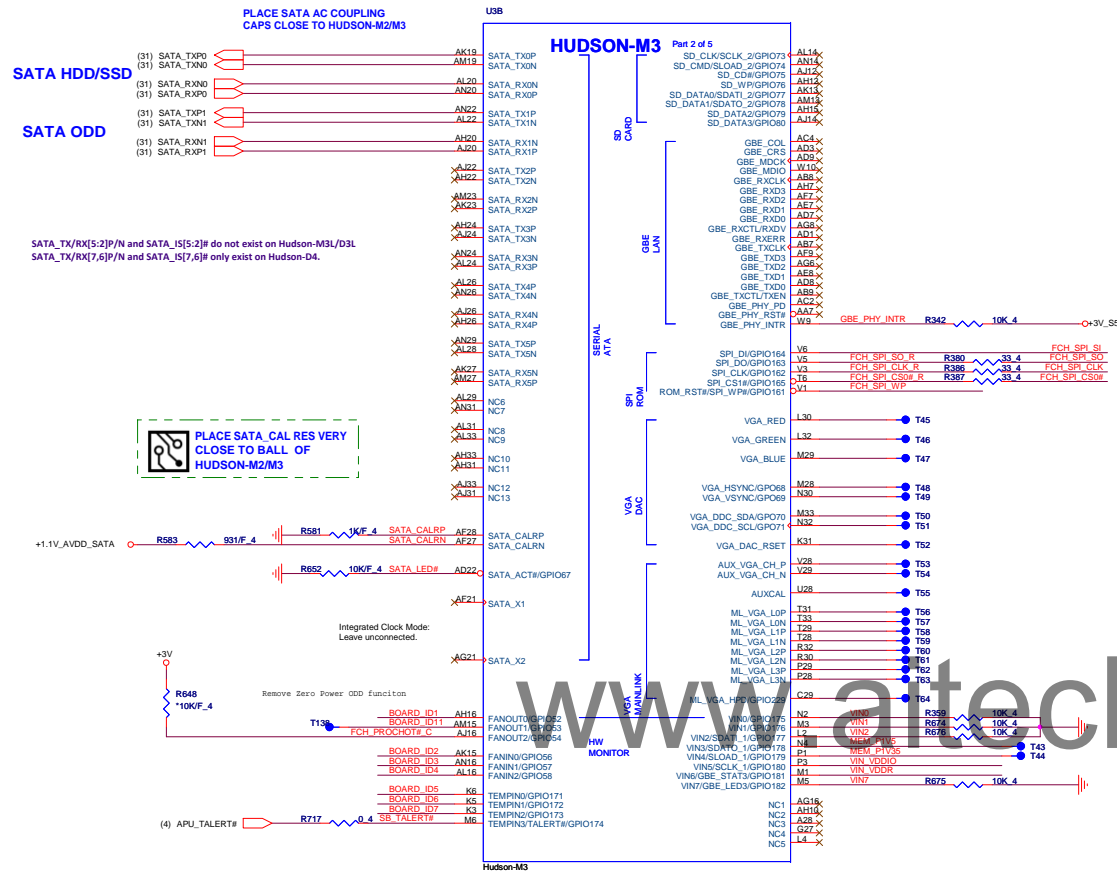
USB3.0 S&C

Note:
SCL2/SDA2: for SMBUS in the S5 power domain
SCL3/SDA3: for SMBUS in the S5 power domain

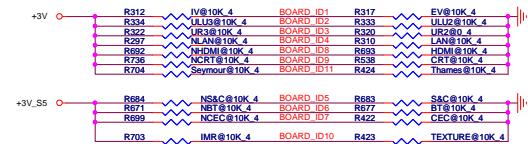
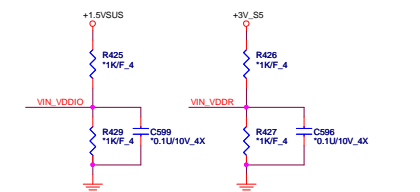
The schematic diagram illustrates the SPI interface between the ATmega328P and the ADXL345. The ATmega328P is shown on the left with pins 18 (SCK), 19 (MISO), 20 (MOSI), and 22 (SS). The ADXL345 is shown on the right with pins 1 (VCC), 2 (GND), 3 (SCL), 4 (GND), 5 (SDA), and 6 (GND). The SCK pin of the ATmega328P is connected to the SCL pin of the ADXL345 through a 10k pull-up resistor (R599) to +3V_S5. The MISO pin of the ATmega328P is connected to the SDA pin of the ADXL345 through a 10k pull-up resistor (R600) to +3V_S5. The MOSI pin of the ATmega328P is connected to the SCL pin of the ADXL345 through a 10k pull-up resistor (R593) to +3V_S5. The SS pin of the ATmega328P is connected to the SDA pin of the ADXL345 through a 10k pull-up resistor (R595) to +3V_S5. The VCC pin of the ADXL345 is connected to +3V_S5 through a 0.4 ohm resistor (R15). The GND pin of the ADXL345 is connected to GND through a 0.4 ohm resistor (R14).

SCL2/SDA2:
SMBUS Implemented: PU 2.2K to +3V_S5
SMBUS Not Implemented: PU 10K to +3V_S5
SCL3/SDA3:
Low Voltage SMBUS Implemented: PU 10K to APU_VDDIO (+3V)
Low Voltage SMBUS Not Implemented: PU 10K to +3V_S5

SPI Shared Flash

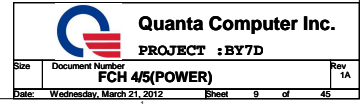


W25Q32BVSSIG:AKE391P0N00
W25Q16BVSSIG:AKE38FP0N01
A-stage Socket: DG008000031 91960-0084L



BOARD ID SETTING

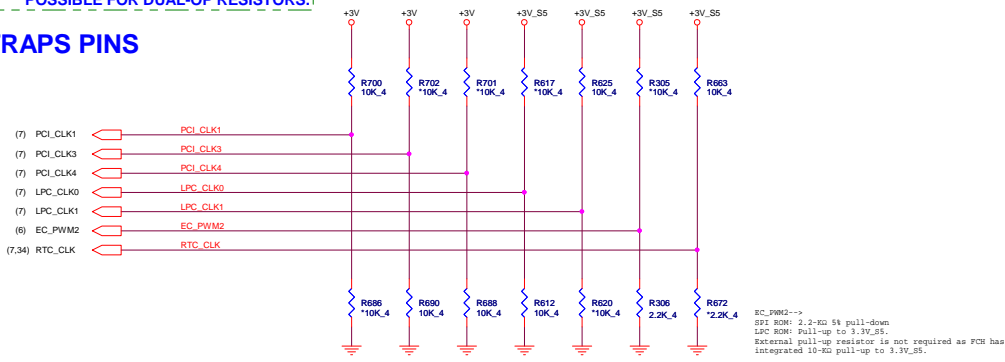
[illegible]





OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

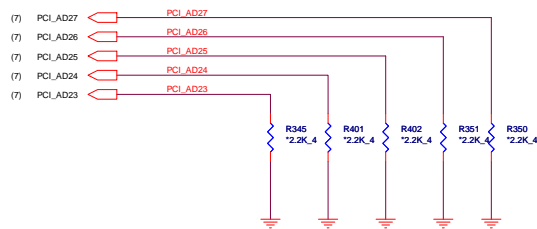


REQUIRED STRAPS

	*****	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	*****	ALLOW PCIE Gen2 DEFAULT	*****	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	*****	FORCE PCIE Gen1	*****	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

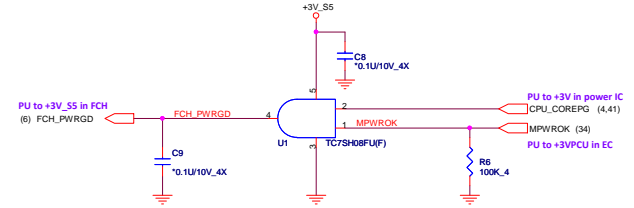
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

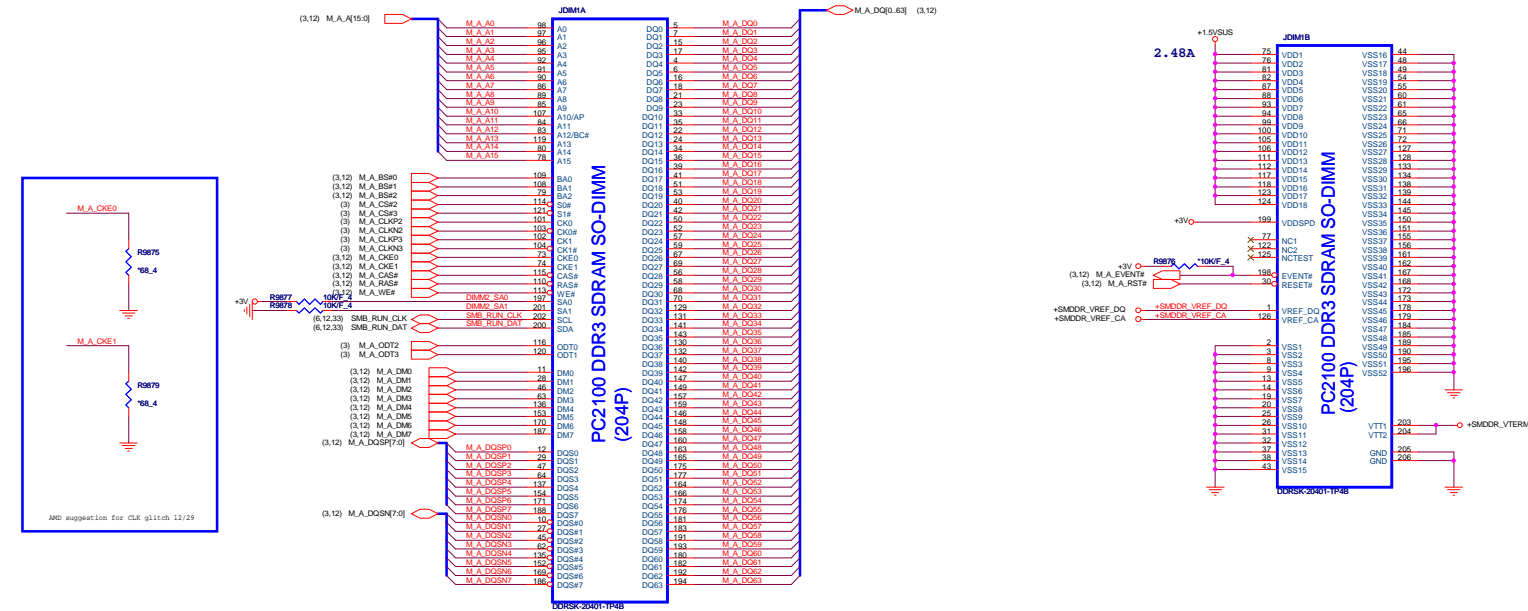


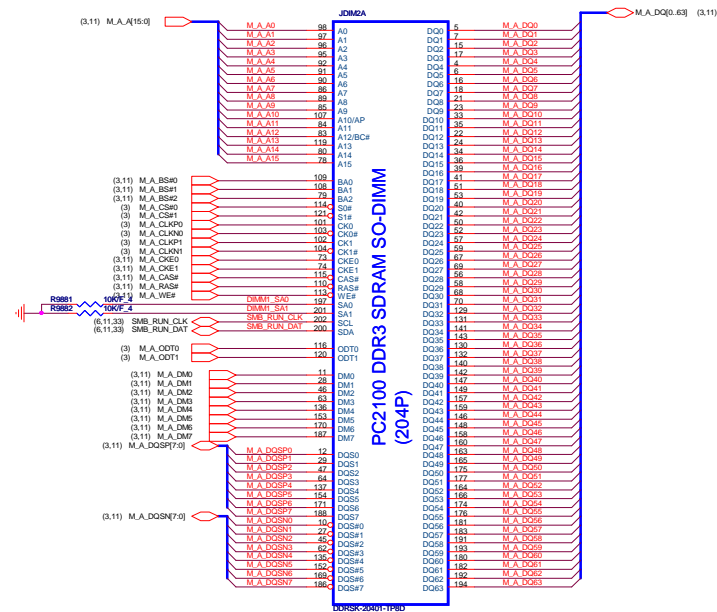
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

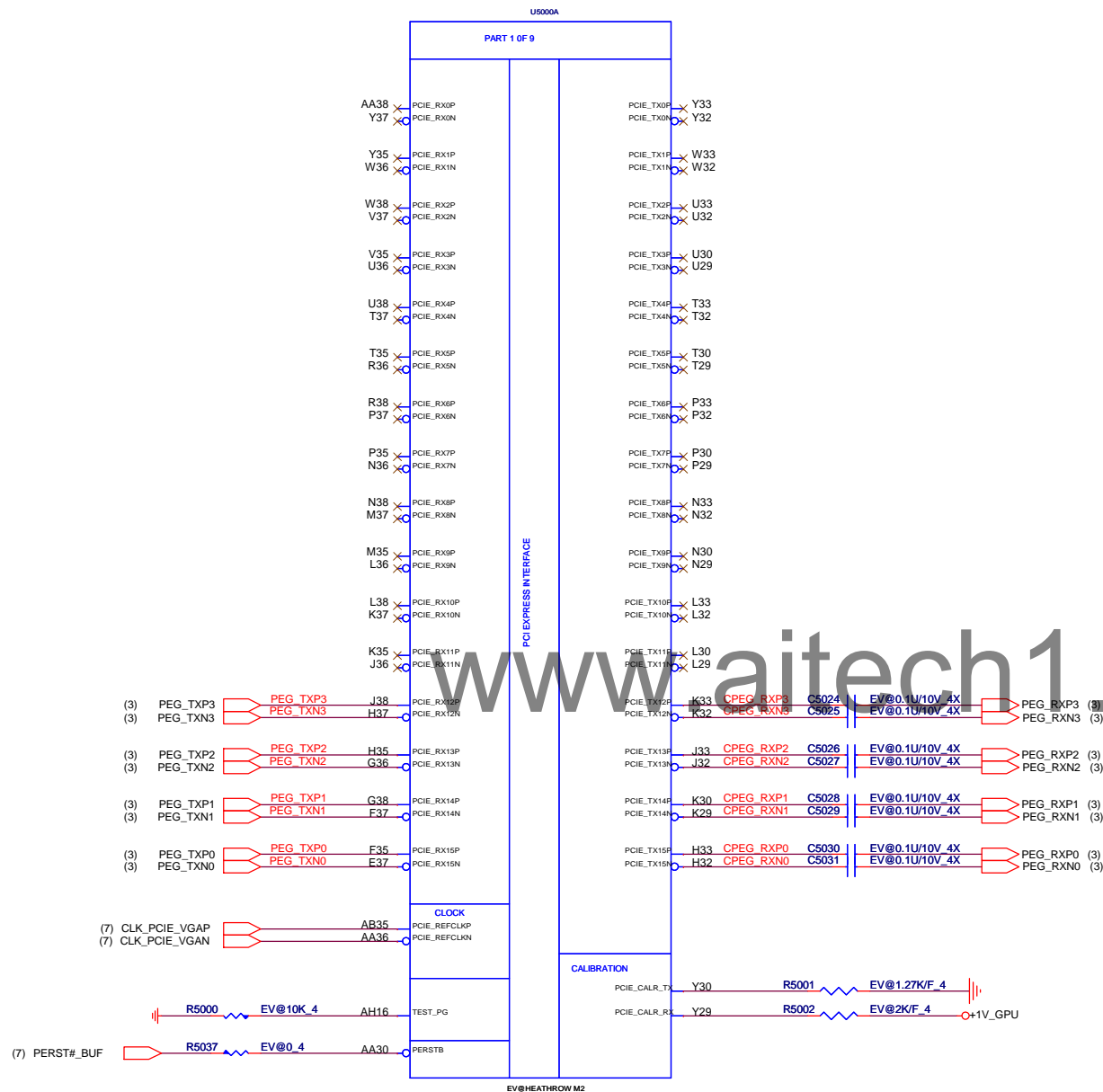
FCH POWER GOOD CIRCUIT



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<Layout Note>
Close to CPU



Seymour Power-on sequence

- 1 => +1V_GPU
- 2 => +3V_GPU
- 3 => +VGPU_CORE,+1.5V_GPU
- 4 => +1.8V_GPU

PEG

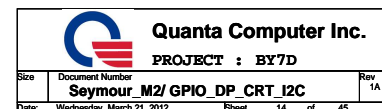
Intel platform: Lane0 ~ Lane15
Brazos platform: Lane12 ~ Lane15
Comal and Sabine platform: Lane8 ~ Lane15

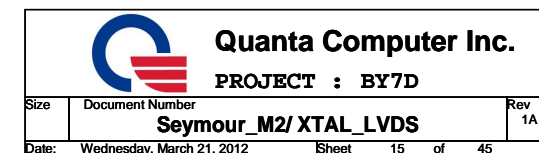


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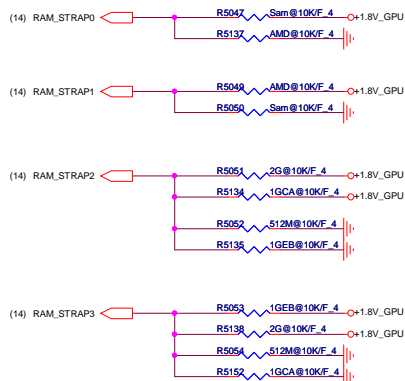
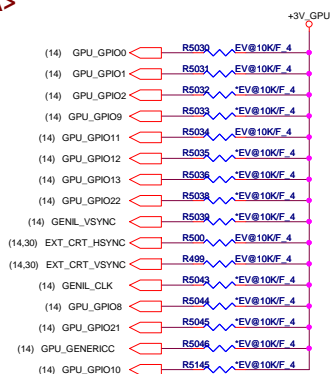
PROJECT : BY7D

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	Seymour_M2/ PEG*16	1A
Date:	Wednesday, March 21, 2012	Sheet 13 of 45





<VGA>



DDR3 Memory TYPE

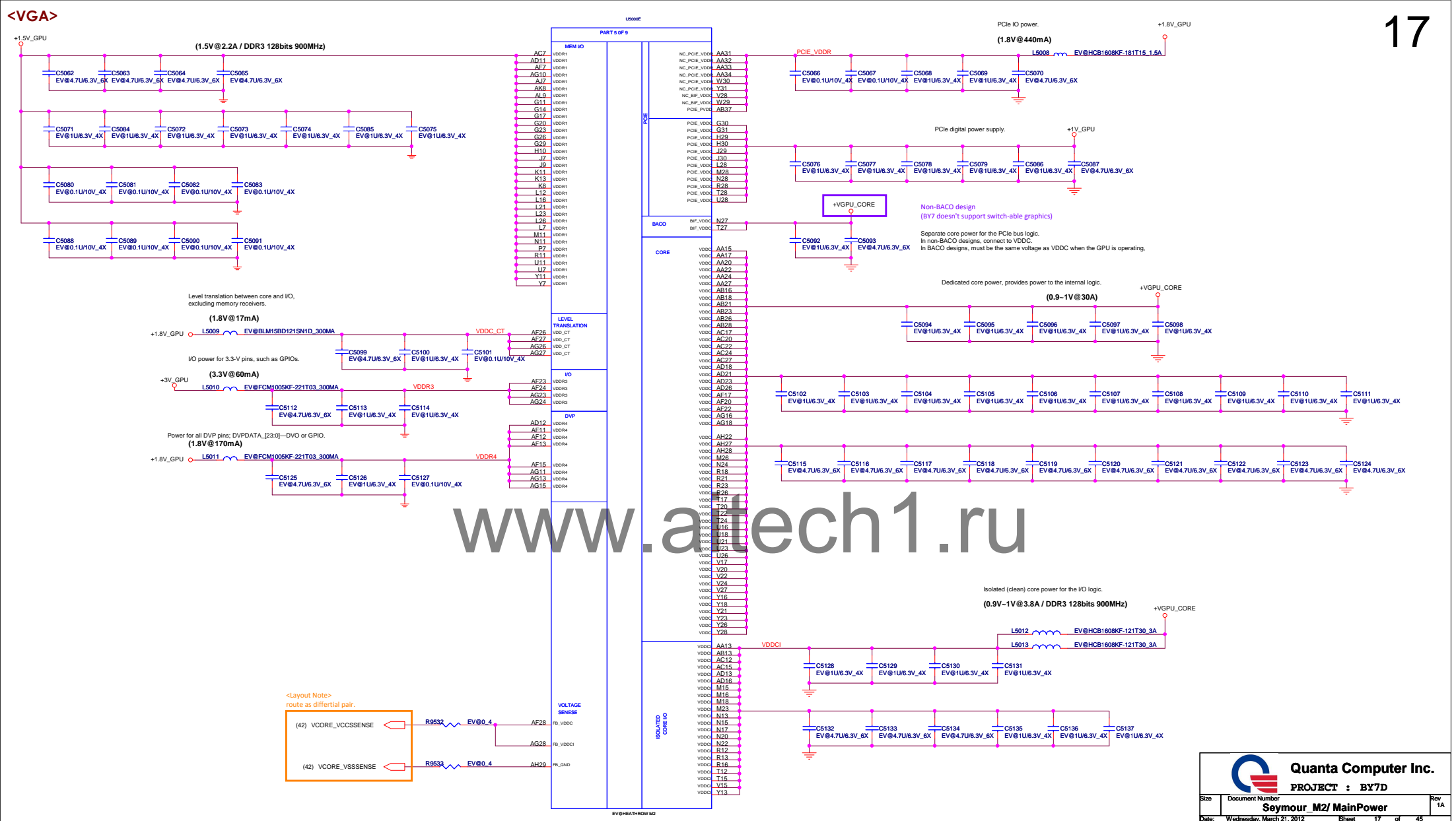
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVDPDATA_3	RAM_STRAP2 DVDPDATA_2	RAM_STRAP1 DVDPDATA_1	RAM_STRAP0 DVDPDATA_0
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 4	512MB	0	0	0	1
	K4W2G1646C-HC11 (128M*16,C-die)	AKD5MGWT500 * 4	1GB	0	1	0	1
	K4W2G1646E-HC11 (128M*16,E-die)	AKD5MGWT500 * 4	1GB	1	0	0	1
	K4W2G1646C-HC11 (128M*16)	AKD5MGWT500 * 8	2GB	1	1	0	1
AMD	23EY2387MC11 (64M*16)	AKD5EZWT700 * 4	512MB	0	0	1	0
	23EY4187MA11 (128M*16,A-die)	AKD5DZWT700 * 4	1GB	0	1	1	0
	23EY4187MB11 (128M*16,B-die)	TBD * 4	1GB	1	0	1	0
	23EY4187MA11 (128M*16)	AKD5DZWT700 * 8	2GB	1	1	1	0

CONFIGURATION STRAPS -- SEE EACH DATABASE FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWR_S_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[6]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERIC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

System Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1

EEPROM

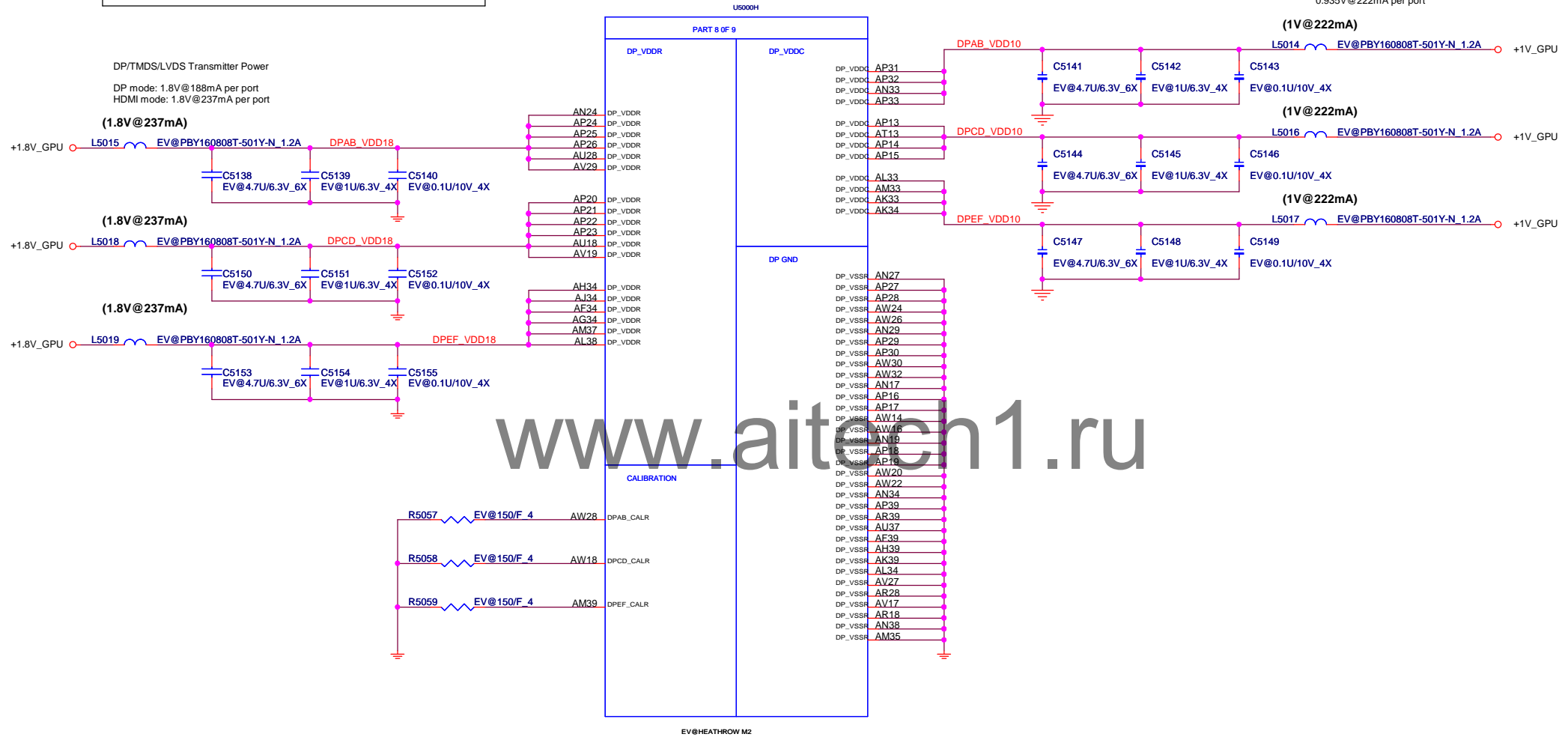


<VGA>

For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

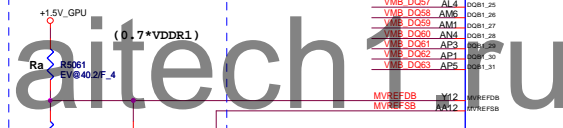


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	Seymour_M2/ DP_Powers	1A
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GPU_DRAM_RST

R5074 EV@10K_4

R5076 EV@4.98K_F_4

C5160 EV@120P/50V_4N

R5075 EV@51F_4

<B3A_20120213>
change R5075 value to 51F_4

MEM_RST# (21,22)

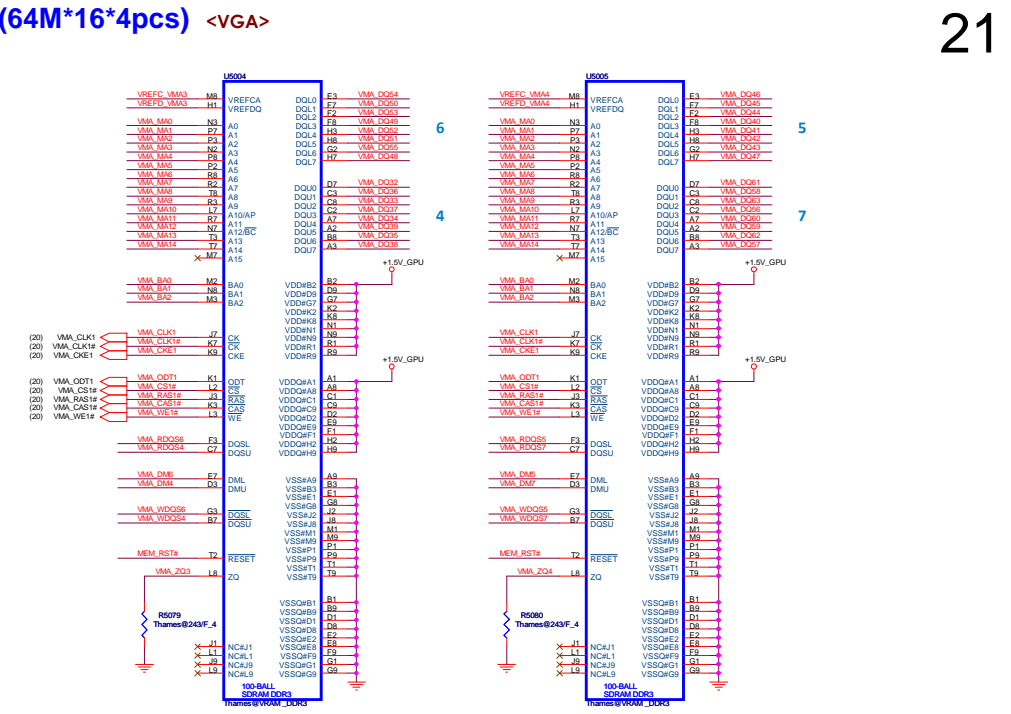
3.3Vdc (pin)

3.3Vdc (pin)

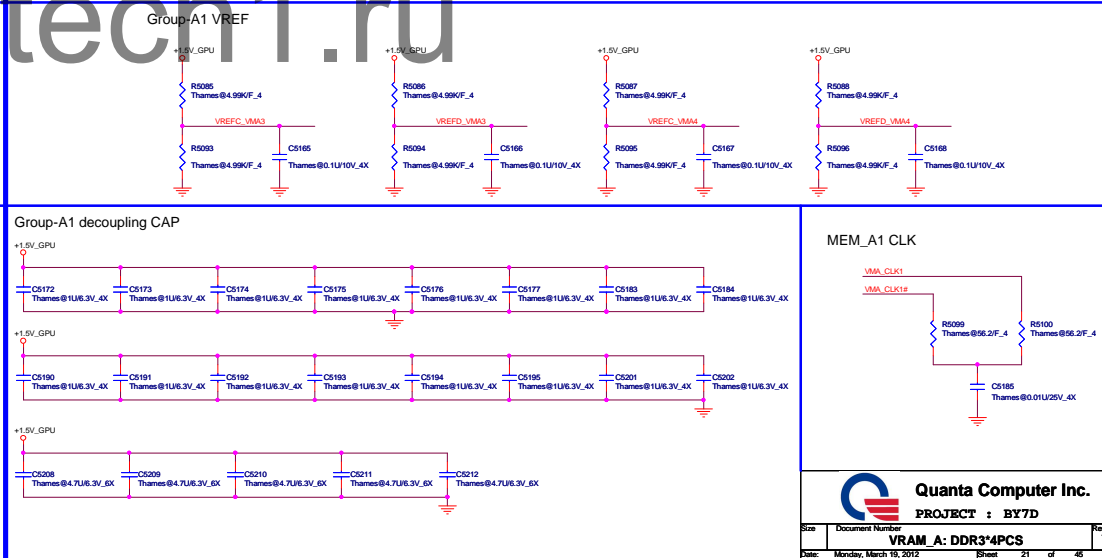
3.3Vdc (pin)

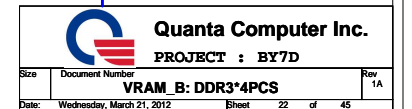
Place all these components very close to GPU (within 25mm) and keep all components close to each other
 * This basic topology should be used for DRAM_RAT for DDR3/GDDR5

These Capacitors and Resistor values are an example only
 The series R and || cap values will depend on the DRAM loads and will have to be calculated for different Memory, DRAM loads and board to pass Reset Signal Spec



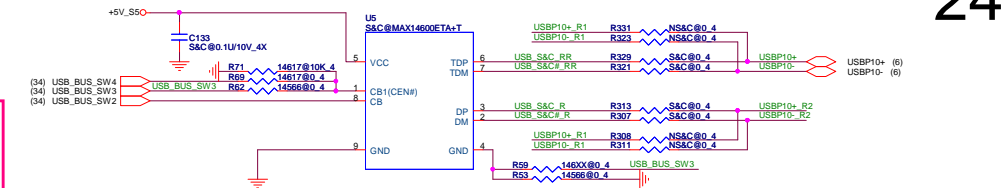
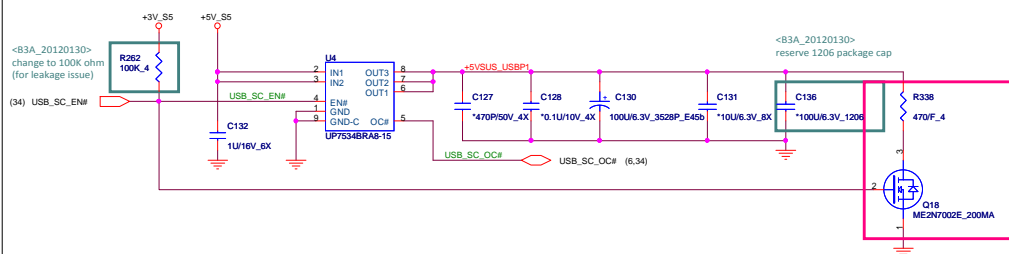
BOT Right





Non-BACO design
(Brazos doesn't support Muxless Switch-able Graphics)

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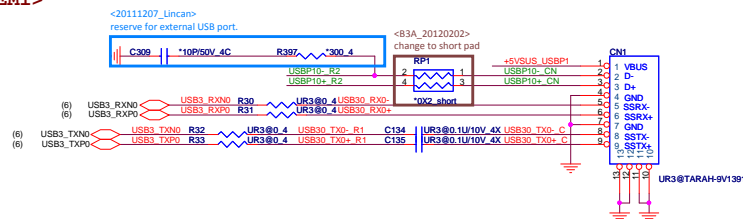
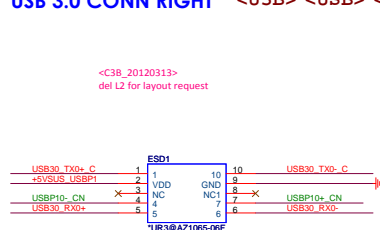


	R69	R62	R59	R53	R7
14566		V		V	
14600			V		
14617(with CB2)	V		V		
14617(no CB2)			V		V

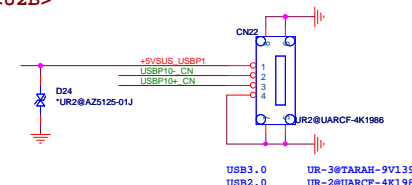
14566/14600		
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM for 14566
1	0	Pass-Through(USB) mode for 14600
1	1	pass-through(USB) with CDP Emulation for 14600

14617				
CB0	CB1	CB2	Status	
X	X	1	Force Apple 2A Charger Mode	
0	0	0	Autodetection charger mode	
0	1	0	Force-Dedicated Charger Mode	
1	0	0	USB Pass-Through Mode Connect DP/DM to TDP/TDM	
1	1	0	USB Pass-Through Mode with CDP Emulation.Auto connect DP/DM to TDP/TDM depending on CDP status	

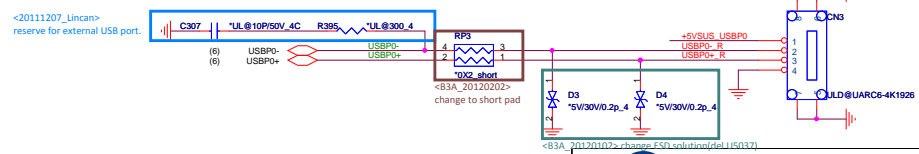
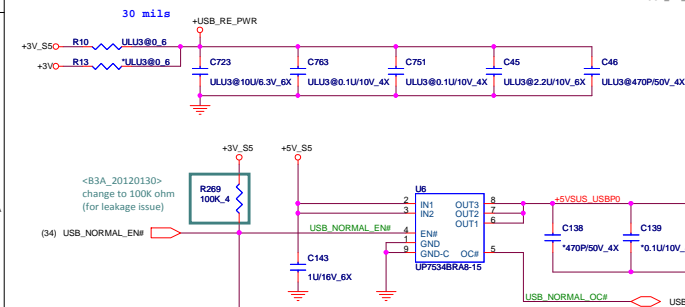
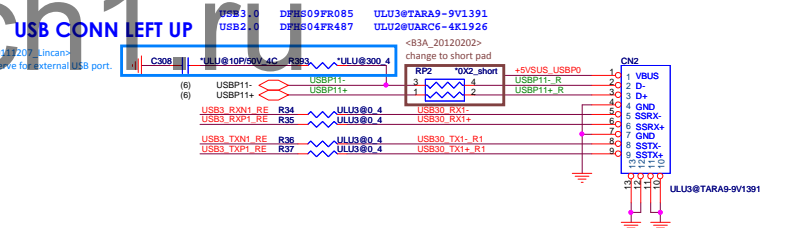
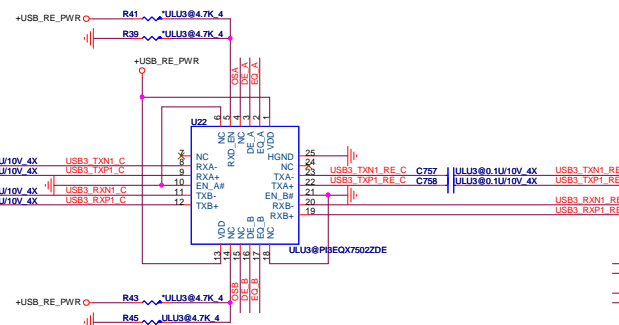
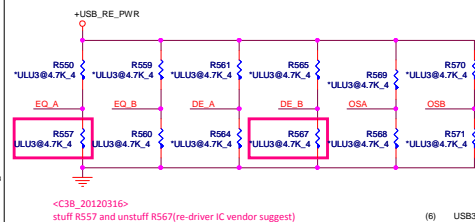
USB 3.0 CONN RIGHT <U3B> <USB> <EMI>

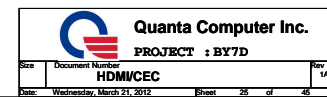


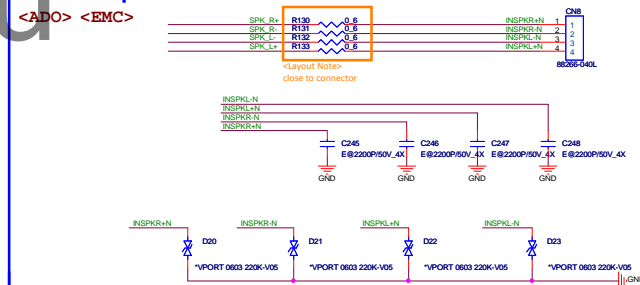
USB 2.0 CONN RIGHT <U3B> <U2B>

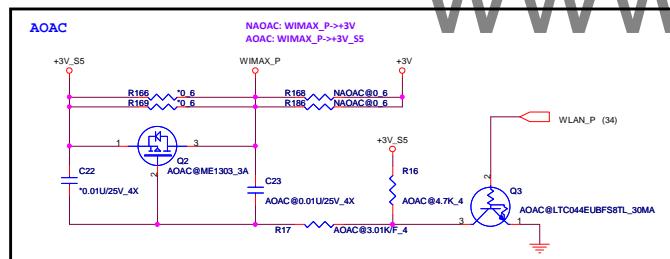
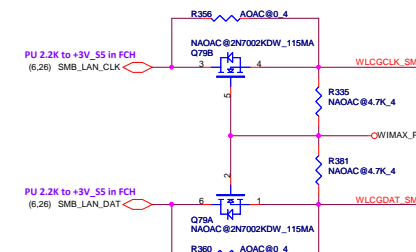


USB 3.0 Power switch





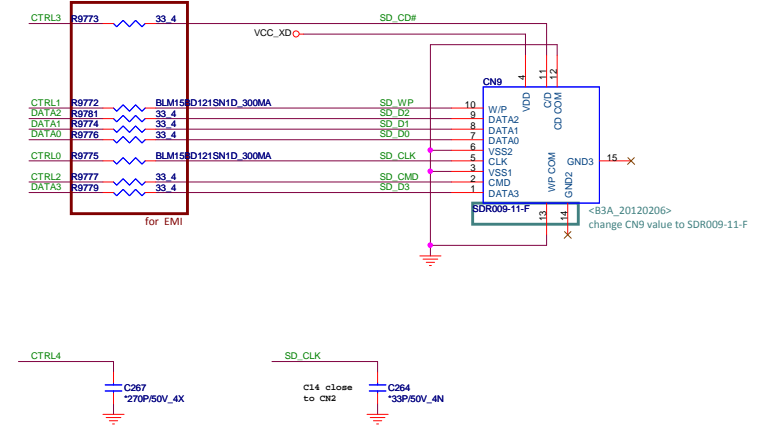




The image shows a detailed PCB layout for the AU6437B53-GDL-QR module. Key components and features include:

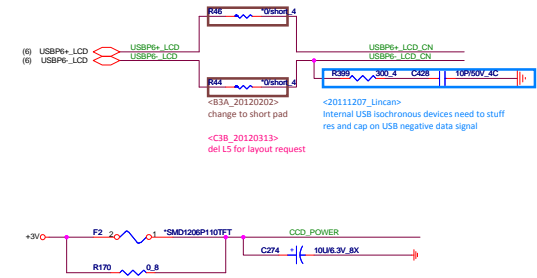
- Connectors:**
 - PLTRST#** (Pin 7): Connected to a 3V supply through a 10k resistor (R147) and a 48M CARD R.
 - USBP5+ / USBP5-** (Pins 6): Connected to a USB port through a 10pF capacitor (C310) and a 300 ohm resistor (R398).
 - 48M CARD R** (Pin 4): A 48M resistor connected to the CARD R pin.
- Resistors:**
 - R148** (0.4 ohms): Connected to the PLTRST# pin.
 - R146** (0.4 ohms): Connected to the 48M CARD R pin.
 - R151** (330.4 ohms): Connected to the 48M CARD R pin.
 - R158** (0.5 short 8): A short circuit connected to the 3V Card pin.
- Capacitors:**
 - C256** (0.1uF/10V/4X): Connected to the 1.8V Card pin.
 - C257** (0.1uF/10V/4X): Connected to the 3V Card pin.
 - C258** (33pF/50V_4N): Connected to the 48M CARD R pin.
 - C259** (1uF/6.3V_4X): Connected to the 3V Card pin.
 - C260** (4.7uF/6.3V_6X): Connected to the 3V Card pin.
 - C261** (4.7uF/6.3V_6X): Connected to the 1.8V Card pin.
 - C262** (0.1uF/10V/4X): Connected to the 3V Card pin.
 - C263** (0.1uF/10V/4X): Connected to the 1.8V Card pin.
- Layout Notes:**
 - "<B3A_20120207> change to short pad"
 - "<B3A_20120207> reserve for external USB port."
 - "<Layout Note> close to IC"
 - "<Layout Note> close to IC"
 - "<Layout Note> close to IC"
- Module Identification:**
 - AU6437B53-GDL-QR**: The main module identifier.
 - 0.5A(30mils)**: A note indicating the current and distance for the 3V Card pin connection.

SD write protect enable
1 : decided by SDWP(default)
0 : SD always write-able

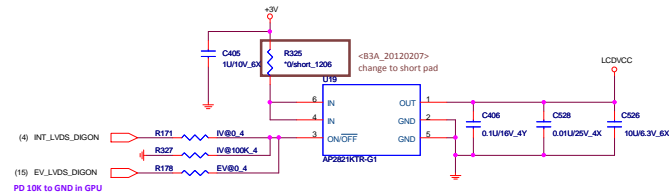


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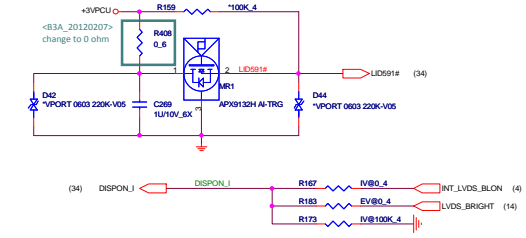
CCD [CCD]



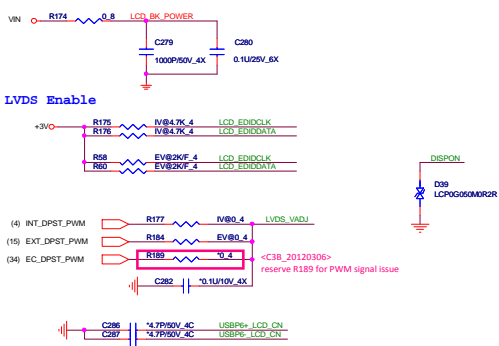
LCD POWER SWITCH <LDS>



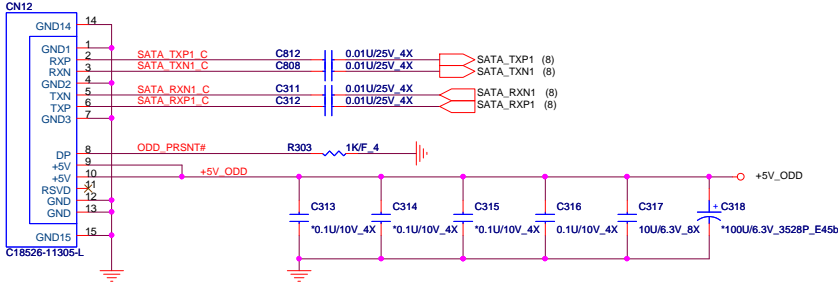
HALL SENSOR&BACK LIGHT SWITCH <HSR>



LCD Panel Module [LDS]



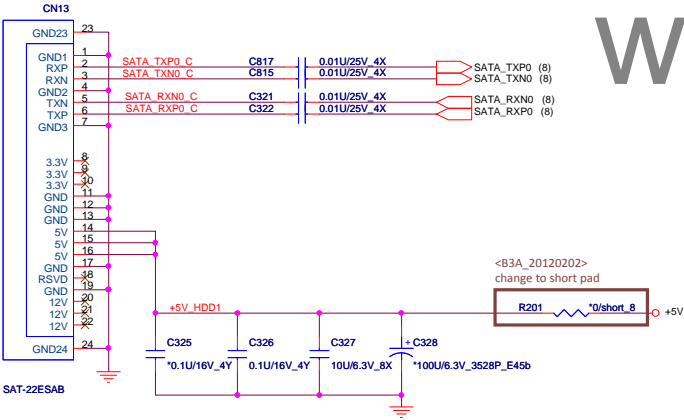
SATA ODD [ODD]



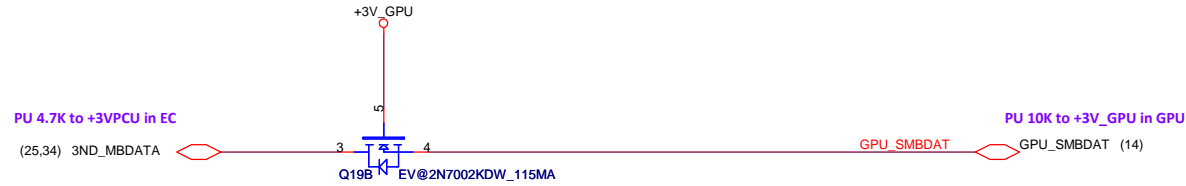
ODD Zero power [OZP]



SATA HDD [HDD]



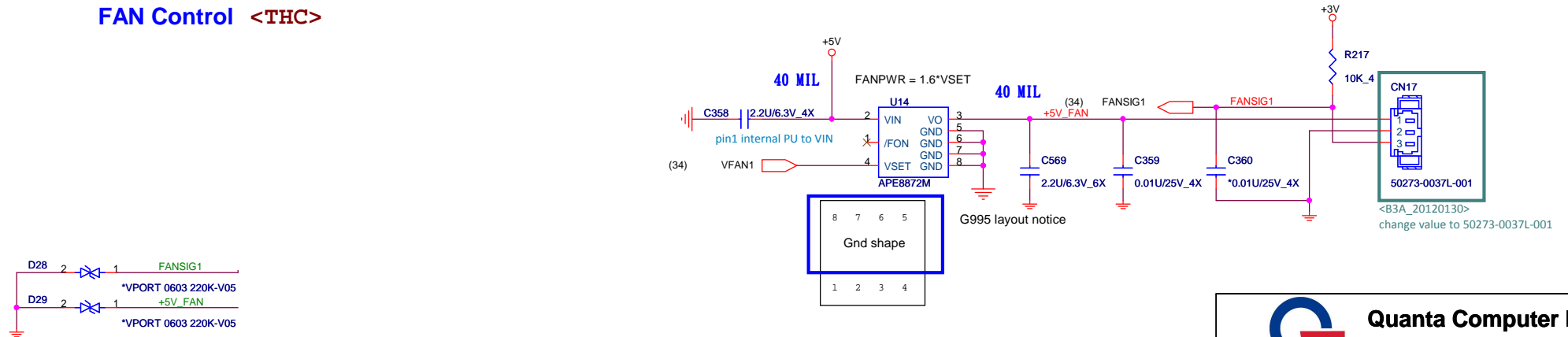
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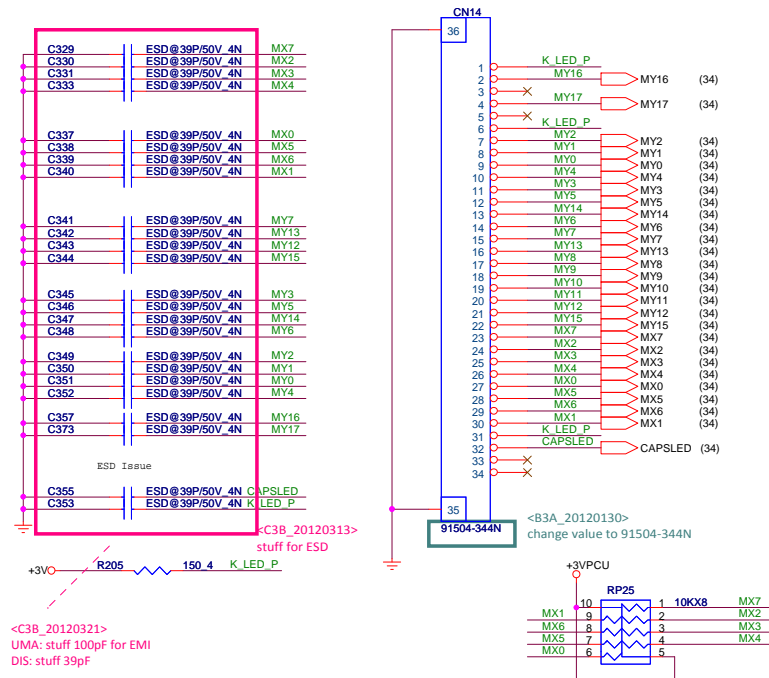
Thermal	dGPU Int Thermal
EC(M) 3ND_SMB	
EC(M) 3ND_SMB	dGPU int SMBUS
dGPU(M) SMB	dGPU int SMBUS

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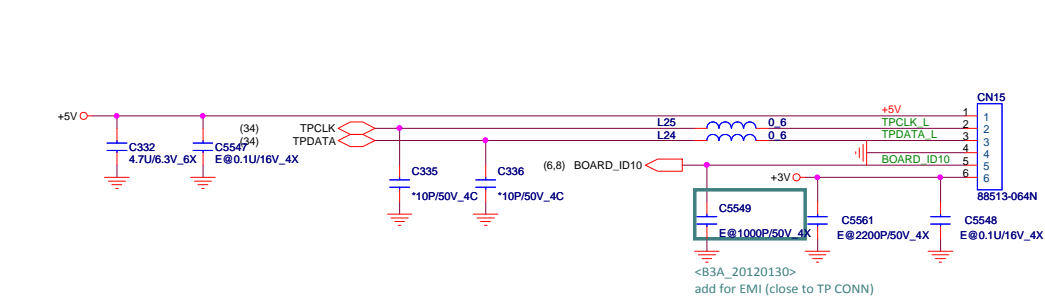
FAN Control <THC>



KEY BOARD Connector <KBC> <EMI>

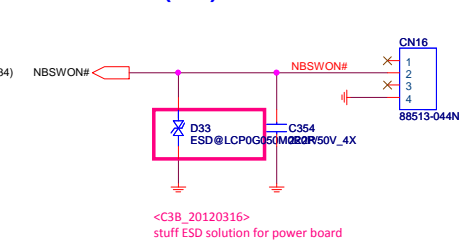


TOUCH PAD BOARD <TPD> <EMI>

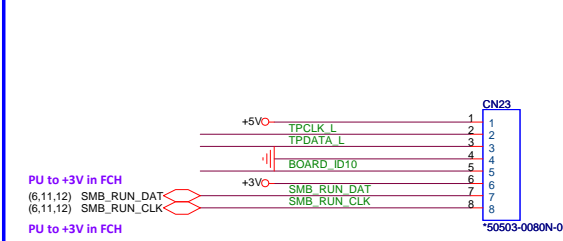


ID_Detect	default
Metal/IMR	H
TEXTURE	L

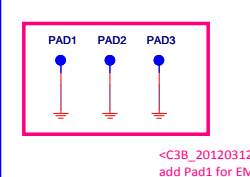
Power Board (UIF) <PSW>



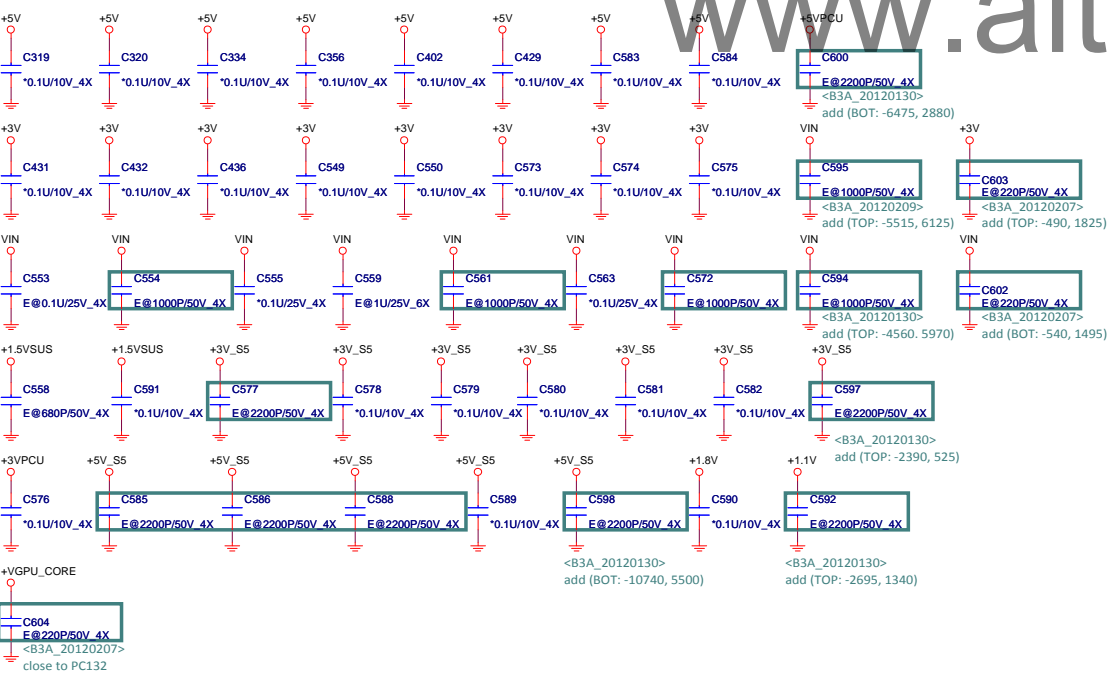
TP board <TPD>



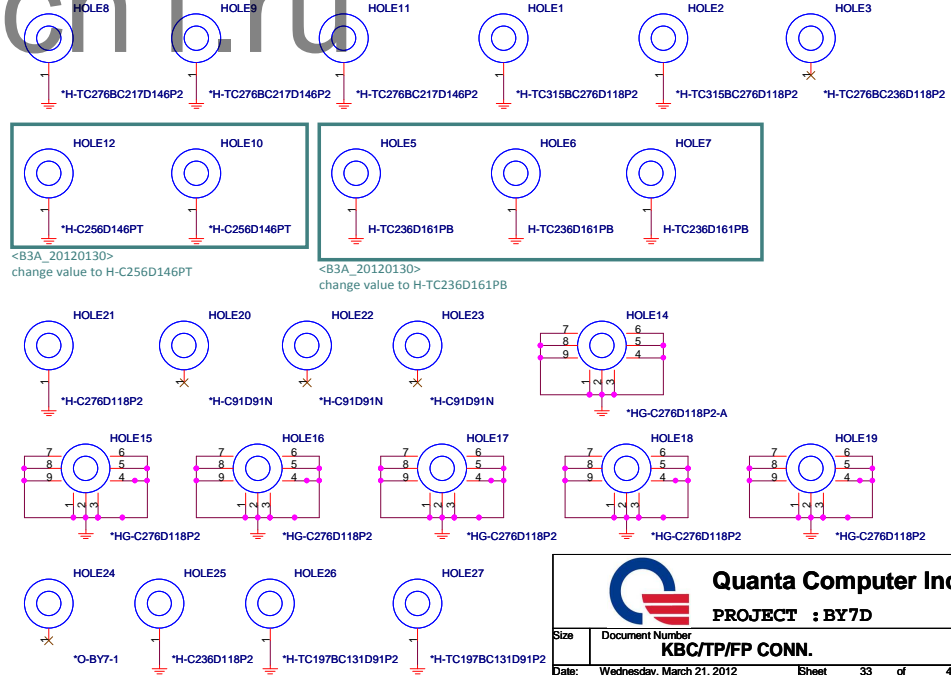
EMI Pad <OTH>

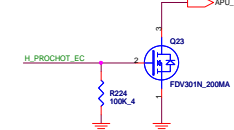
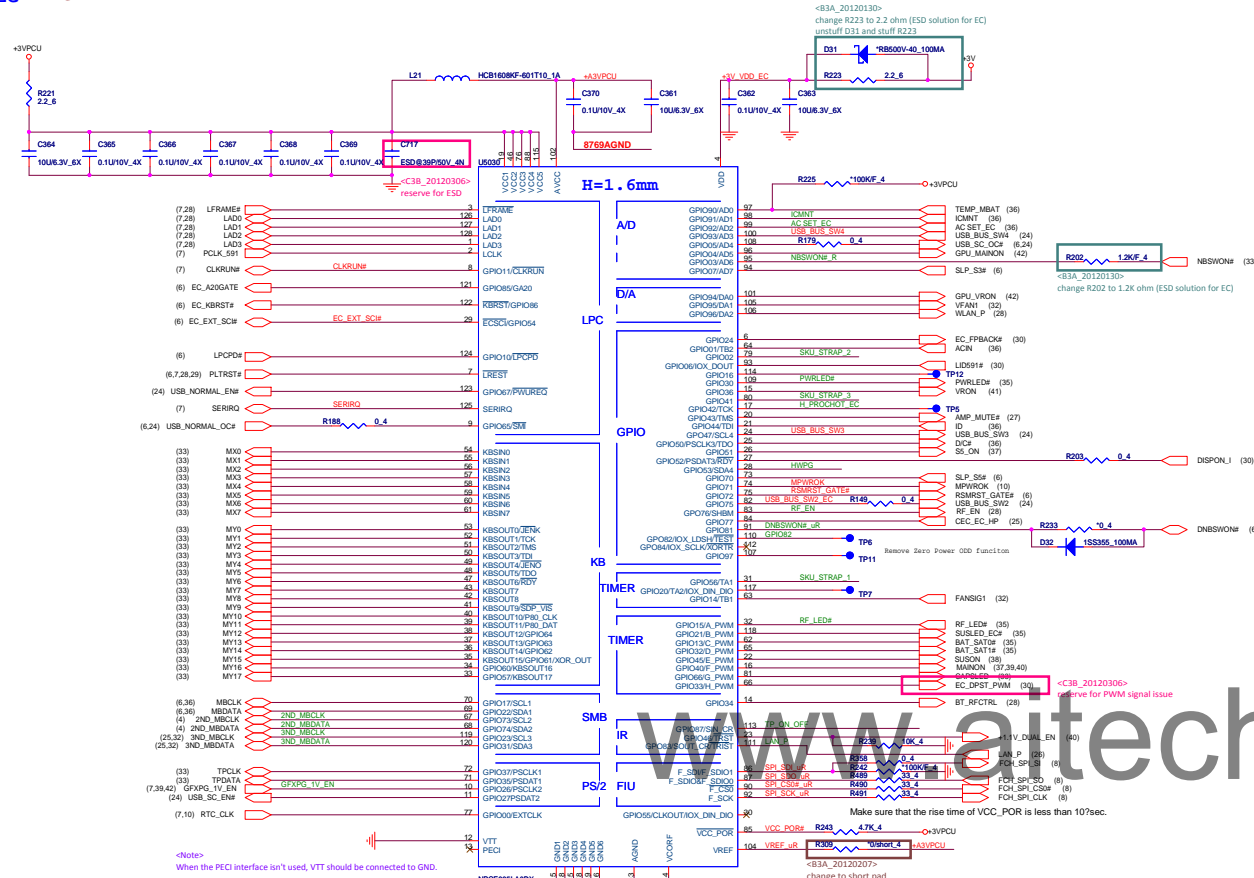


EMI PAD <EMI>

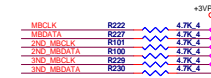


HOLE <OTH>





SM BUS PU <KBC>



SMBus Table

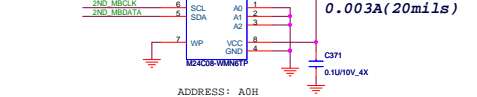
SMBUS	Devices	Address
1	Battery	
2	PCB SML1	
	3D Sensor	32H
	EC EEPROM	A0H
	VGA Board Thermal Sensor	98H
3	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H

Strap <KBC>

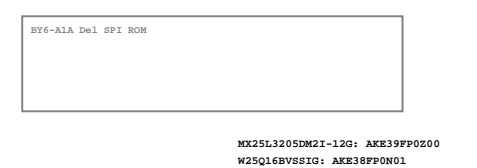
SHBM

SHBM# Enable shared memory with host BIOS
Disabled (1) if using FWH device on LPC
Enabled (0) if using SPI flash for both system BIOS and EC firmware

ID EEPROM <KBC>



SPI FLASH <KBC>

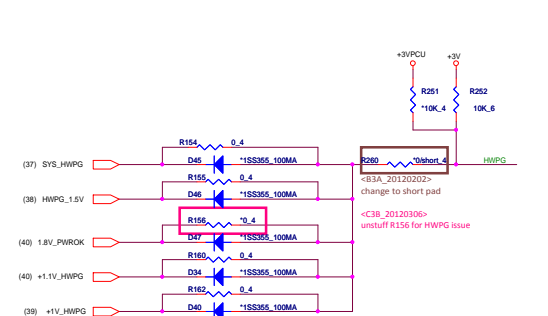


INTERNAL KEYBOARD STRIP

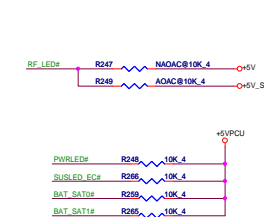
<KBC>



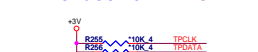
HWP circuit <KBC>



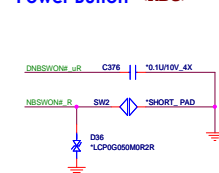
LED PU/PD <LED>



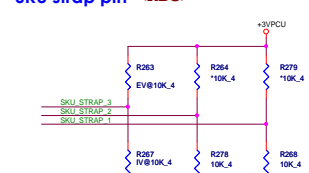
TP interface PU <KBC>



Power Button <KBC>



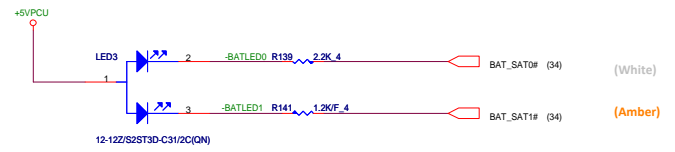
SKU strap pin <KBC>



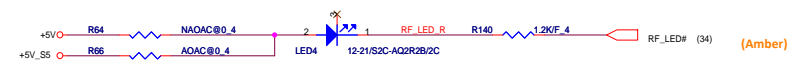
SKU_STRAP_1 (GPIO56)	SKU_STRAP_2 (GPIO02)	SKU_STRAP_3 (GPIO41)	SKU
0	0	0	Brazos UMA
0	0	1	Brazos DIS
0	1	0	COMAL UMA
0	1	1	COMAL DIS
1	0	0	Deccan UMA
1	0	1	Deccan DIS

LED <LED>

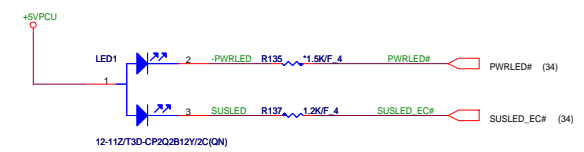
BATTERY



RF LED <LED>

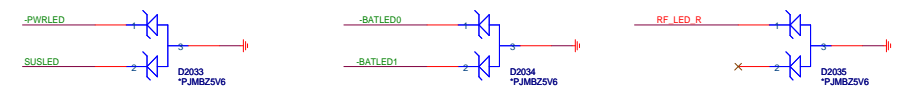


POWER <LED>

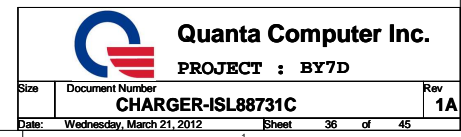


LED P/N	Behavior	res
BEWY0007ZA0 (White/Amber)	power on: White LED bright sleep: Amber LED blink	R135: stuff 1.5K R137: stuff 1.2K
BEWH0051Z00 (White)	power on: White LED bright sleep: White LED blink	R135: unstuff R137: stuff 1.5K

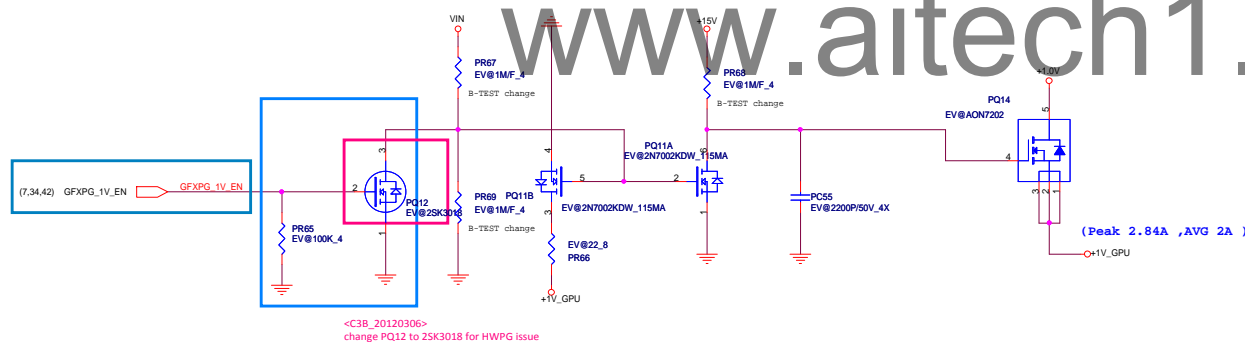
ESD Protect <ESD>

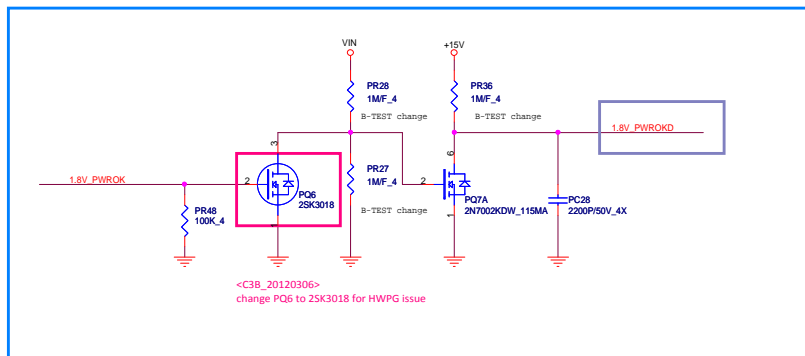
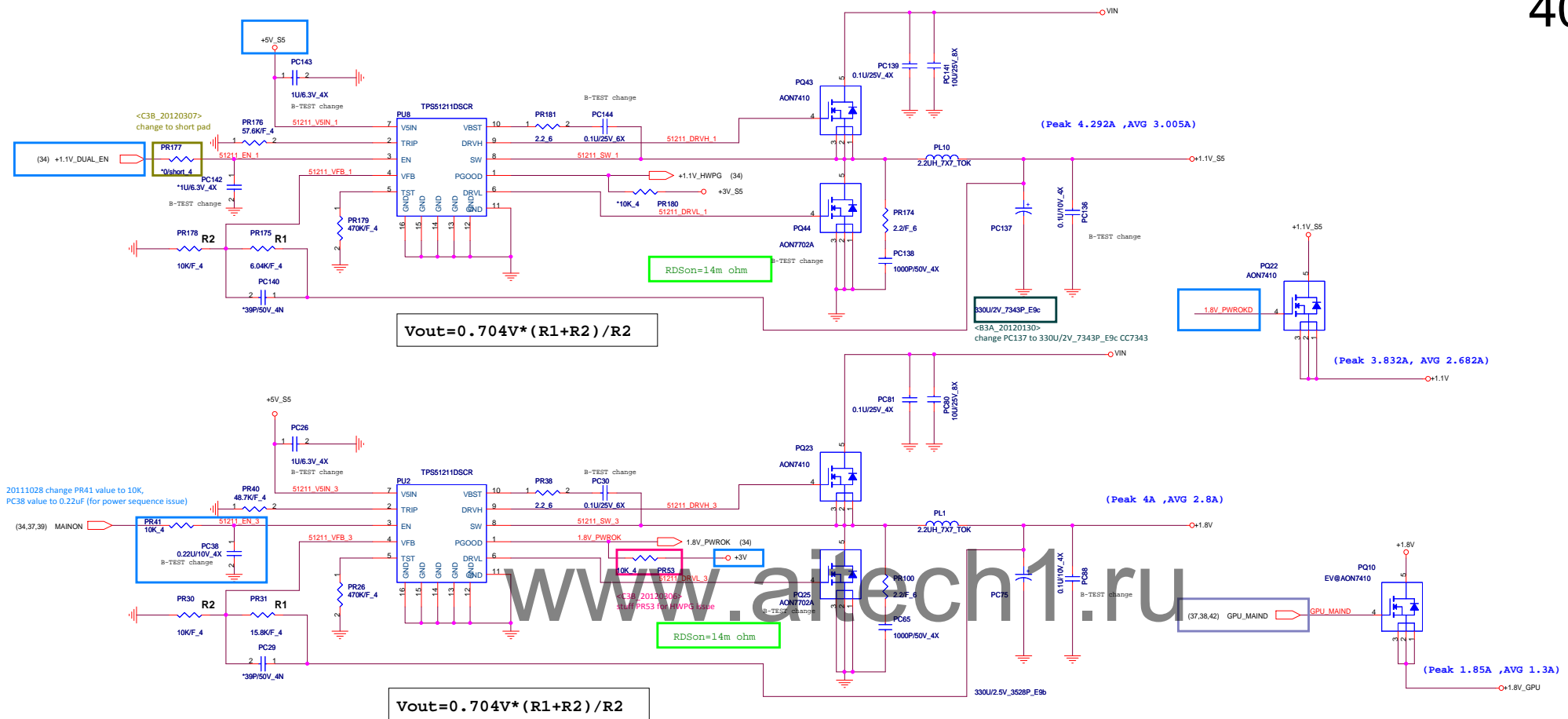


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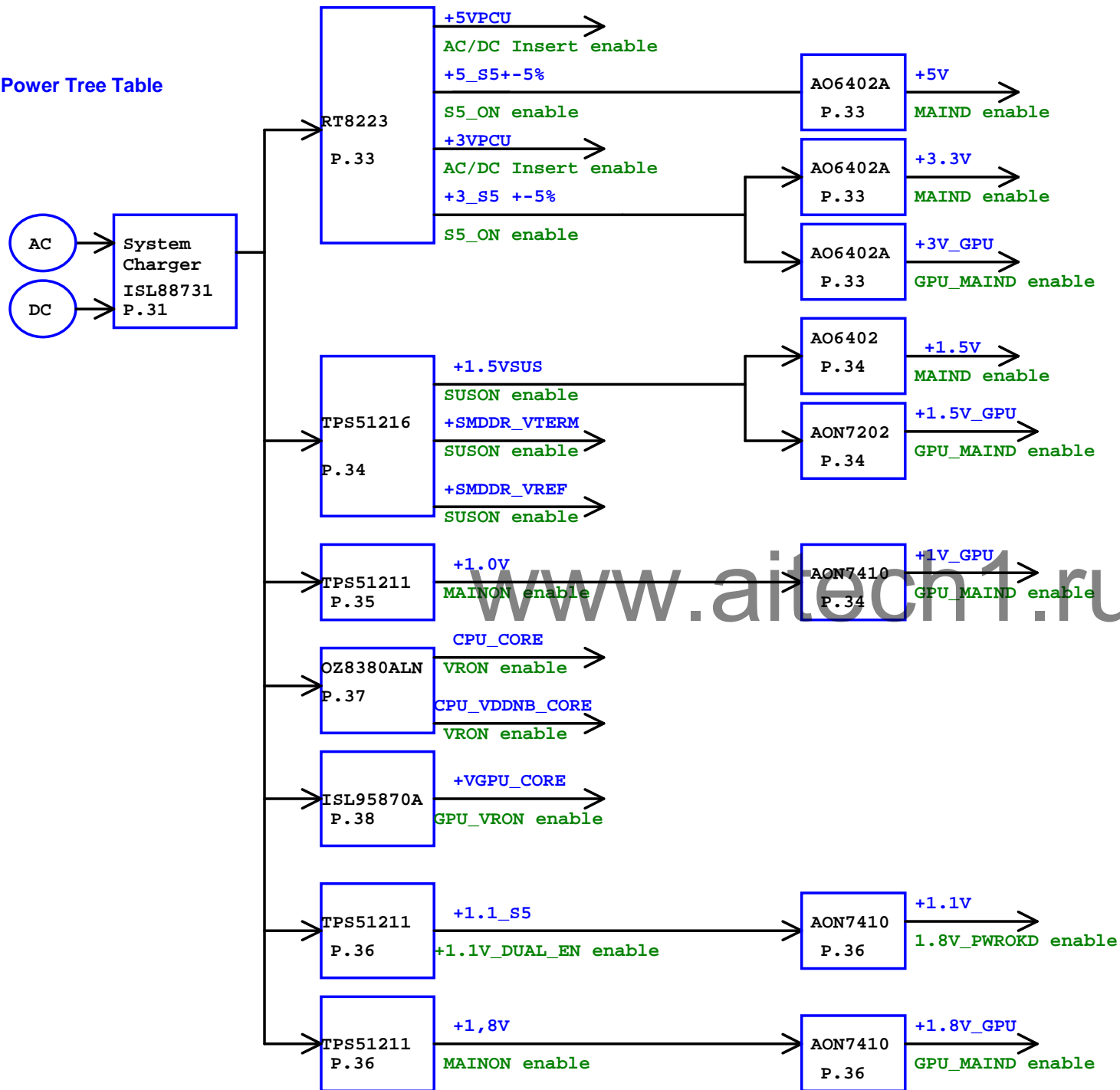




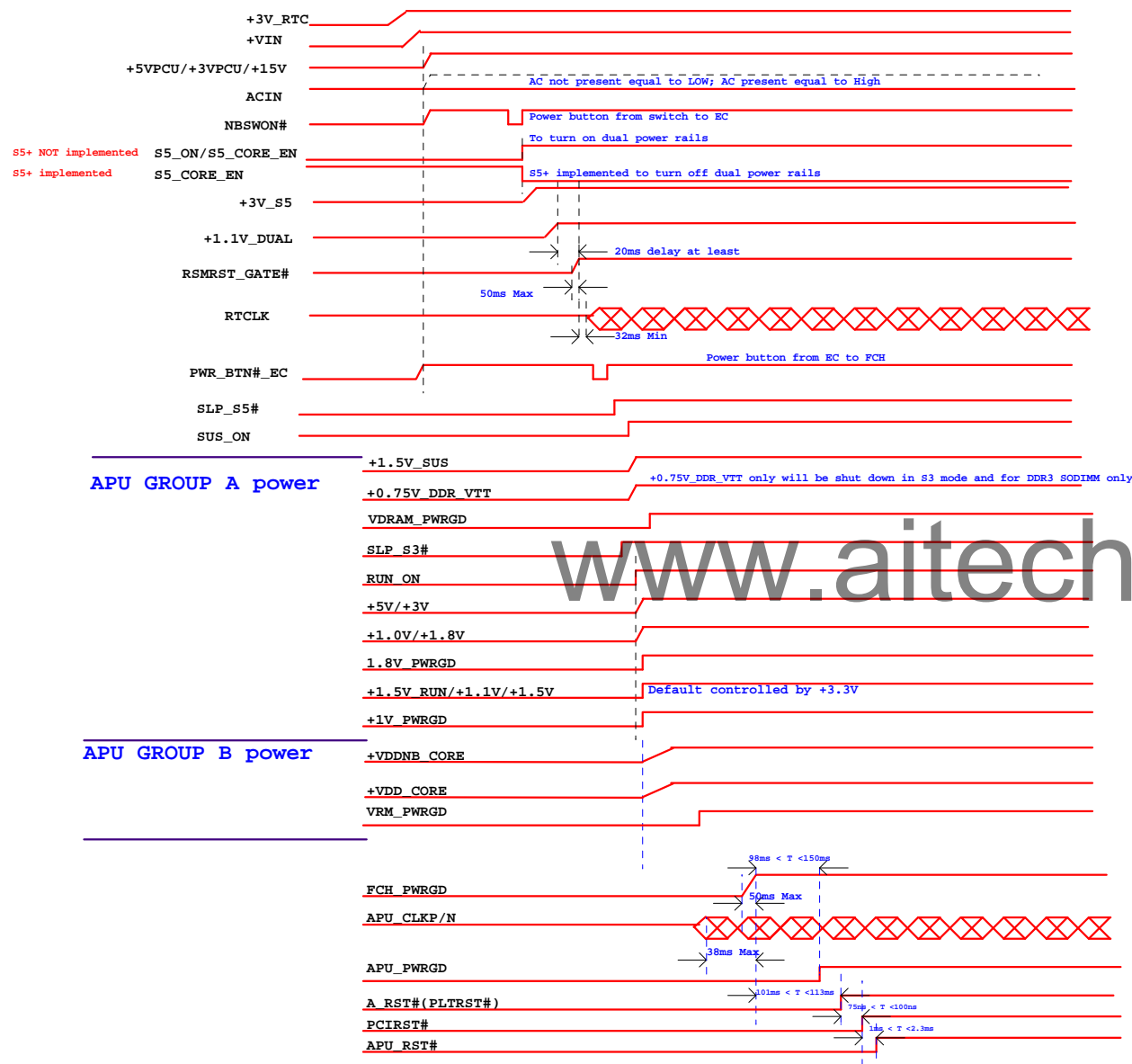


	Seymour
R1	60.4K/F_4
R2	31.6K/F_4
R3	590K/F_4
R4	294K/F_4
R5/R6	3.65K/F_4
R7/R8	4.3K/F_4

Power Tree Table



BY7D Power On Sequence: S5 > S0



APU Power on sequence required:

APU:

1.GROUP A(VDD10,VDD18, VDDIO, VDD33)ramp before GROUP B(VDDCR,VDDNB)

HUDSON-M2/M3:

1.+3V_S5 ramp before +1.1V_DUAL

2.+3V ramp before +1.1V

3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Seymour XT S3 package Power-on sequence

All power rails reach nominal within 20ms

1=> +3V_GPU

2=> +VGPU_CORE/+1V_GPU

3=> +VGPU_CORE PWRGD to enable +1.5V_GPU

4=> +1V_GPU PWRGD to enable +1.8V_GPU

NOTE

1.+3V to turn on +3V_GPU

2.+3V_GPU ready to enable +VGPU_CORE/+1V_GPU
(+1V_GPU will ramp up before +VGPU_CORE)

3.+VGPU_CORE PWRGD to enable +1.5V_GPU

3.+1V_GPU PWRGD to enable +1.8V_GPU

[illegible]